RealWear: Improving Performance and Lifetime of SSDs Using a NAND Aging Marker

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Outline

➢ NAND aging marker of a flash storage system
   ❑ Wear mechanism of NAND flash memory
   ❑ Inadequacy of the conventional P/E cycle-based NAND aging marker

➢ RealWear: New NAND aging marker
   ❑ Design of RealWear
   ❑ Model Calibration
   ❑ Validation of RealWear: Lifetime, Error variations, Self-recovery effect

➢ Impact of RealWear: Three case studies

➢ Conclusions
NAND Flash Memory 101

Single NAND flash cell

Vcg (>20V)

Control Gate
 Blocking Oxide
 SiN layer

Source
 e-
 e-

Drain
 e-
 e-

Vsub (>20V)

Tox

Probability

Lowest Voltage State

Read Reference Voltage (R1)

P1

MSB

01

LSB

Read Reference Voltage (R2)

P2

10

Read Reference Voltage (R3)

P3

00

Threshold Voltage Distribution

Threshold Voltage

ER

11
High operating voltage (> 20V) damages the tunnel oxide, and generates traps in the tunnel oxide.

Repeated program & erase operation (P/E cycles) wear-out NAND flash memory because of tunnel oxide degradation.
Wear Mechanism of NAND Flash Memory

NAND flash operations are similar to those of paper: Write, Read, Erase
Similar to paper, when NAND flash memory experience “write and erase” (i.e., P/E cycles) repeatedly, it is worn-out
Inadequacy of P/E Cycle-based NAND Aging Marker

- **The most common wear indicator is to count the chronological age of a NAND cell based on the number of program/erase cycles.**

**Conventional P/E cycle-based NAND aging marker is not sufficient to indicate the wear status of individual NAND flash blocks.**

Performance’20 | 7

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Why P/E Cycle-based NAND Aging Marker is Inadequacy?

- P/E cycle-based NAND aging marker is similar as the chronological age of a human being.

Human

- Genetic difference (Telomere)

NAND block

- “Process variations”
- “Operating Conditions”

Even twins, human can exhibit different aging characteristics

Chronological age: 33
Biological age: 20

Chronological age: 45
Biological age: ??

Even twins, human can exhibit different aging characteristics

Life style or living environments

Process variations

Operating Conditions
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Goal of Our New NAND Aging Marker: RealWear

- Conventional P/E cycle-based NAND aging marker

- New NAND aging marker to accurately indicate the wear status of NAND blocks
RealWear: Design Methodology

- **RealWear considers multiple variables that are closely related to the wear-out of NAND flash memory.**

  ✓ Variables selection using real state-of-the-art 3D TLC flash chips + Regression model

**Phase 1: Variable Selection**

- (Evaluation) 48-layer 3D TLC chips
- Flash Controller
- Temp. Controller and Cooler

**Phase 2: Building Model**

- (Correlation analysis)
- Key variables

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We conducted the correlation test between 12-month retention bit errors after the maximum P/E cycles, N(12), cycles and each variables.

We conducted the correlation test between 12-month retention bit errors after the maximum P/E cycles, N(12), cycles and each variables using lifetime evaluations and using a **regression model**.
RealWear: Variable Selection

- Investigated 10 candidate variables and selected 5 variables for RealWear based on the correlation with the wear status of flash blocks

<table>
<thead>
<tr>
<th>Type</th>
<th>Description</th>
<th>Inclusion</th>
</tr>
</thead>
<tbody>
<tr>
<td>Latency</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tPROG</td>
<td>Program latency</td>
<td>X</td>
</tr>
<tr>
<td>tBERS</td>
<td>Erase latency</td>
<td>O</td>
</tr>
<tr>
<td>tREAD</td>
<td>Read latency</td>
<td>X</td>
</tr>
<tr>
<td>Bit errors</td>
<td>N(0) # of bit errors right after program</td>
<td>O</td>
</tr>
<tr>
<td>Noise factors</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ICI</td>
<td>Inter-Cell Interference</td>
<td>X</td>
</tr>
<tr>
<td>RTN</td>
<td>Random Telegraph Noise</td>
<td>X</td>
</tr>
<tr>
<td>BPD</td>
<td>Back Pattern Dependency</td>
<td>X</td>
</tr>
<tr>
<td>Dynamic factors</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N_{P/E}</td>
<td>P/E cycles</td>
<td>O</td>
</tr>
<tr>
<td>D_{t}</td>
<td>Dwell time</td>
<td>O</td>
</tr>
<tr>
<td>K_{amb}</td>
<td>Ambient temperature</td>
<td>O</td>
</tr>
</tbody>
</table>

Not correlated in high-endurance region

Difficult to on-line measure
RealWear: Building Model

- RealWear is constructed by multiple variables using regression model.

$$f(x) = C_0 + \beta_1 \cdot N_{PE} + \beta_2 \cdot tBERS + \beta_3 \cdot N(0) + \beta_4 \cdot \ln(D_t^{eff})$$

Each coefficients were estimated by least square approximation method.

- $tBERS$,
- $RBER$,
- # of P/E cycles
- Dwell time,
- Ambient temperature

On-line measurable variables related to the wear of NAND flash memory
The effectiveness of RealWear was verified over P/E cycle-based aging marker by:

- 1. How accurately it can estimate the lifetime of each NAND blocks
- 2. How effectively it can reduce the error variations between NAND blocks
- 3. How well it can reflect the effect of operating conditions on the wear of NAND flash memory (i.e., self-recovery effect)

\[
\text{Life} = \frac{\text{Predicted total amounts of writes}}{\text{Actual total amounts of writes}} \times 100
\]

Unlike P/E-cyle based NAND aging marker, RealWear can accurately indicate the real lifetime of NAND blocks.
Model Validation: Error Variations

- The effectiveness of RealWear was verified over P/E cycle-based aging marker by:
  
  2. How effectively it can reduce the error variations between NAND blocks

Unlike P/E-cycle based NAND aging marker, NAND blocks with the same RealWear values exhibit almost the same number of bit errors.
Model Validation: Operating Condition Effects

- The effectiveness of RealWear was verified over P/E cycle-based aging marker by:
  
  ✓ 3. How well it can reflect the effect of operating conditions on the wear of NAND flash memory (i.e., self-recovery effect)

Unlike P/E-cycle based NAND aging marker, RealWear properly reflects the impact of I/O workload variation and temperature variation on the wear of NAND blocks.
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  □ Model Calibration
  □ Validation of RealWear: Lifetime, Error variations, Self-recovery effect

➢ Evaluation: Results of three case studies

➢ Conclusions
Experiment Settings

- **RealWear-aware flash transition layer (rftl)** is implemented based on a flash emulation environment.

![Diagram of RealWear-aware FTL](image)

**RealWear-aware FTL (rftl)**

- L2P Mapping Table
- Garbage Collector
- Wear Leveler
- Block Age Manager
- Flash Controller
- 3D TLC NAND Flash Memory

- 576 pages per block
- 16-KiB page size

**Characteristics of six workload**

<table>
<thead>
<tr>
<th>Workload</th>
<th>Read:Write</th>
<th>WAF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Varmail</td>
<td>40:60</td>
<td>2.7</td>
</tr>
<tr>
<td>Fileserver</td>
<td>40:60</td>
<td>5.4</td>
</tr>
<tr>
<td>Proxyserver</td>
<td>55:45</td>
<td>1.9</td>
</tr>
<tr>
<td>Webserver</td>
<td>85:15</td>
<td>1.2</td>
</tr>
<tr>
<td>OLTP</td>
<td>70:30</td>
<td>2.0</td>
</tr>
<tr>
<td>NTRX</td>
<td>5:95</td>
<td>2.3</td>
</tr>
</tbody>
</table>
Case Study 1: Lifetime

- **We measured the total amount of writes until an SSD reaches the end of its lifetime.**

- **rftl** can serve on average 63% more writes over the baseline FTL. (max. by 12 times).
**Case Study 2: Performance (Overhead of Garbage Collection)**

- `rftl` can maximize the effect of the existing optimization technique.

- `rftl` can improve the flash performance by reducing the GC overhead (~21%)
Case Study 3: BoundedRead (Read latency Improvement)

- To minimize the fluctuations in read latency, the optimal read reference voltage is provided as look-up table depending on the wear status of NAND blocks.

<table>
<thead>
<tr>
<th>P/E = 8000</th>
<th>1day → 365day</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1</td>
<td></td>
</tr>
<tr>
<td>:</td>
<td></td>
</tr>
<tr>
<td>R7</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>P/E = 100</th>
<th>1day → 365day</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1</td>
<td></td>
</tr>
<tr>
<td>:</td>
<td></td>
</tr>
<tr>
<td>R7</td>
<td></td>
</tr>
</tbody>
</table>

**ORT_pe**

(optimal read reference table based on # of P/E cycles)

**ORT_pe**

(optimal read reference table based on RealWear)

VS.

<table>
<thead>
<tr>
<th>RealWear = 1.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1</td>
</tr>
<tr>
<td>:</td>
</tr>
<tr>
<td>R7</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>RealWear = 0.1</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1</td>
</tr>
<tr>
<td>:</td>
</tr>
<tr>
<td>R7</td>
</tr>
</tbody>
</table>
Case Study 3: BoundedRead (Read latency Improvement)

- **In ORT_rw, no blocks need more than 2 read retries regardless of the data retention requirement.**

  ✓ Using 160 read 3D TLC flash chips

**ORT_pe @8,000 P/E cycles**

**ORT_rw @8,000 P/E cycles**

Case Study 3: BoundedRead (Read latency Improvement)

- rftl can effectively mitigate the fluctuations in read latency

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**rftl** can bound the read latency within 3 tR even at the end of lifetime of NAND flash-based storages.
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Conclusions

- Conventional P/E cycle-based NAND aging marker is not sufficient to indicate the wear status of NAND flash memory
  → Process variation between NAND blocks & different operating conditions

- Presented a new NAND aging marker, RealWear, and verified its adequacy by comparing it with other existing NAND aging markers.
  - Implemented using multiple NAND parameters & validated using read 160 3D TLC flash chips
  - Improving lifetime (63% on average, max 12 times), reducing GC overhead (21%), and mitigating the read latency fluctuations

- Future Directions
  - ML-based Aging Marker Development
  - Real-Time SSD based on Bounded Reads
Thank You!
Bit Errors Due to Wear of NAND Flash Memory

- As NAND flash memory wear-out, Vth distributions of the NAND flash cells are widen and shifted, thus generating NAND bit errors.

✓ NAND bit errors cause a long read latency due to read retires
✓ If NAND bit errors exceeds ECC capability even after read retries, NAND blocks is regarded as bad block (failure)
Why P/E Cycle-based NAND Aging Marker is Inadequacy?

- There are several factors to affect the wear status of NAND flash memory.

### Process variation effect

WL Gate = 30V

NAND cell (a)

- tox 6nm
- Substrate

50MV/cm stress

### I/O workload & Operating environment effect

WL Gate = 30V

NAND cell (b)

- tox

50MV/cm stress

- time T with no operations

To reflect various factors to cause difference aging characteristics in NAND blocks, we propose a new NAND aging marker.

- "Self-Recovery Effect"
- Traps are degenerated by thermal energy

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The Results of Correlation Test
The Results of Correlation Test

- **Graph 1**: Comparison of ICI and BPD with $\Delta V_{th}$ [mV] vs. N(12).
- **Graph 2**: Box plot of $\Delta$ Read Errors vs. N(12).
- **Graph 3**: Histogram of N(12) for 3K P/E cycles and 8K P/E cycles vs. $D_t$ [min.].
- **Graph 4**: Bar graph showing number of 10 P/E cycles with different dwell times and temperatures.