RealWear: Improving Performance and Lifetime of SSDs Using a NAND Aging Marker

Myungsuk Kim, Myoungjun Chun, Duwon Hong,

Yoona Kim, Geonhee Cho, Dusol Lee, and Jihong Kim

Department of Computer Science and Engineering, Seoul National University

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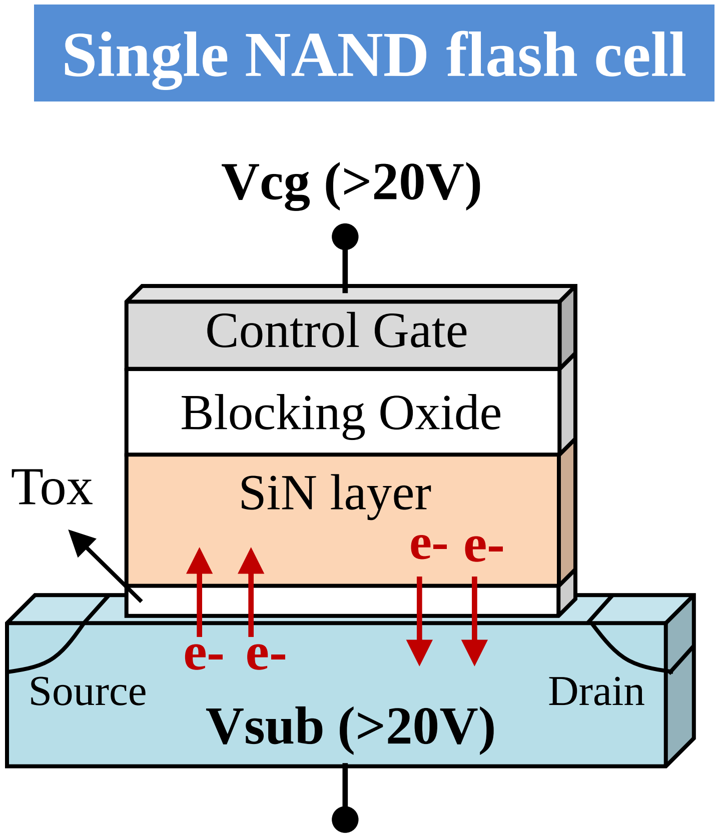
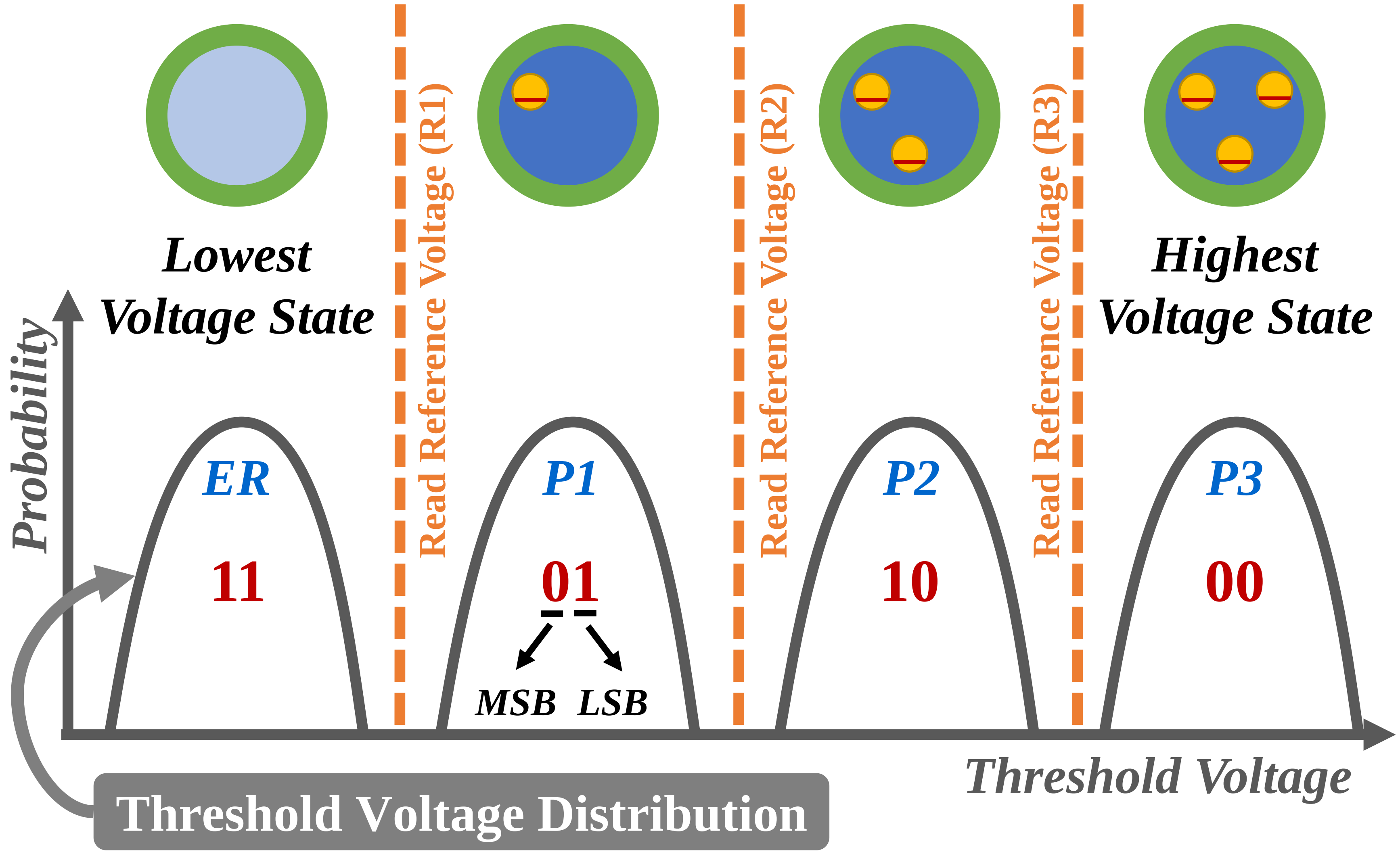
Outline

- **NAND aging marker of a flash storage system**
  - Wear mechanism of NAND flash memory
  - Inadequacy of the conventional P/E cycle-based NAND aging marker
- **RealWear: New NAND aging marker**
  - Design of RealWear
  - Model Calibration
  - Validation of RealWear: Lifetime, Error variations, Self-recovery effect
- **Impact of RealWear: Three case studies**
- **Conclusions**

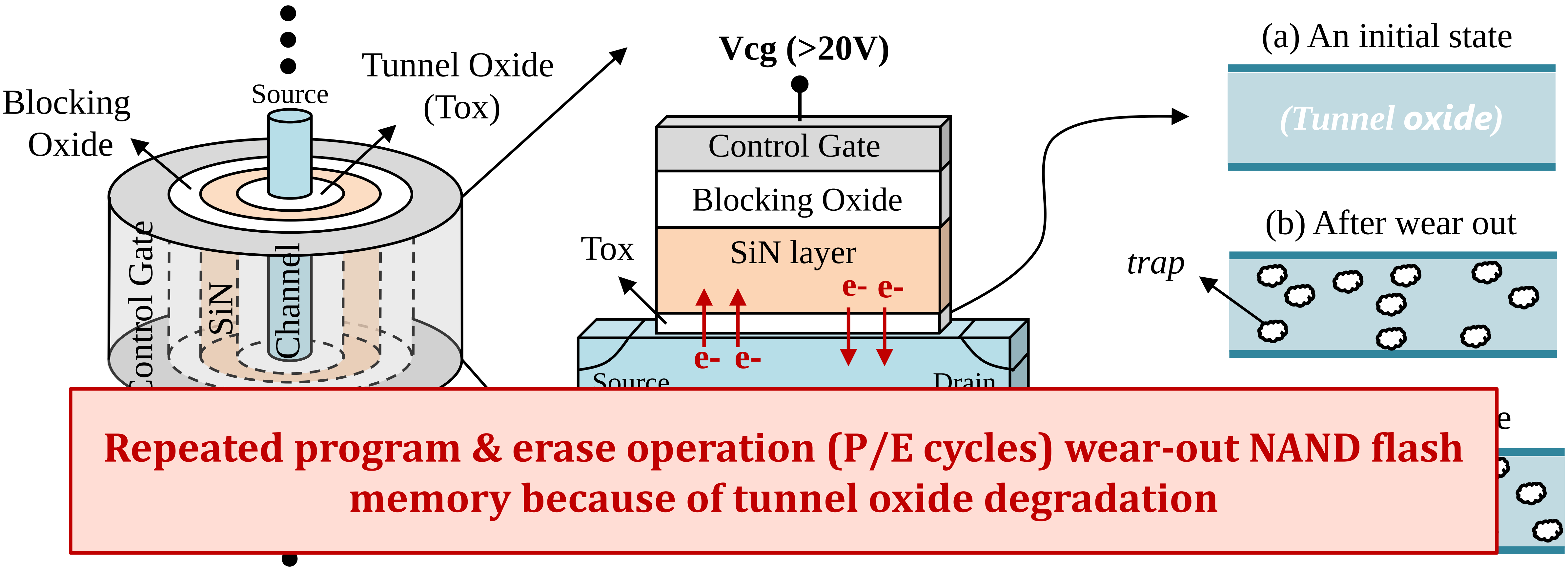
NAND Flash Memory 101





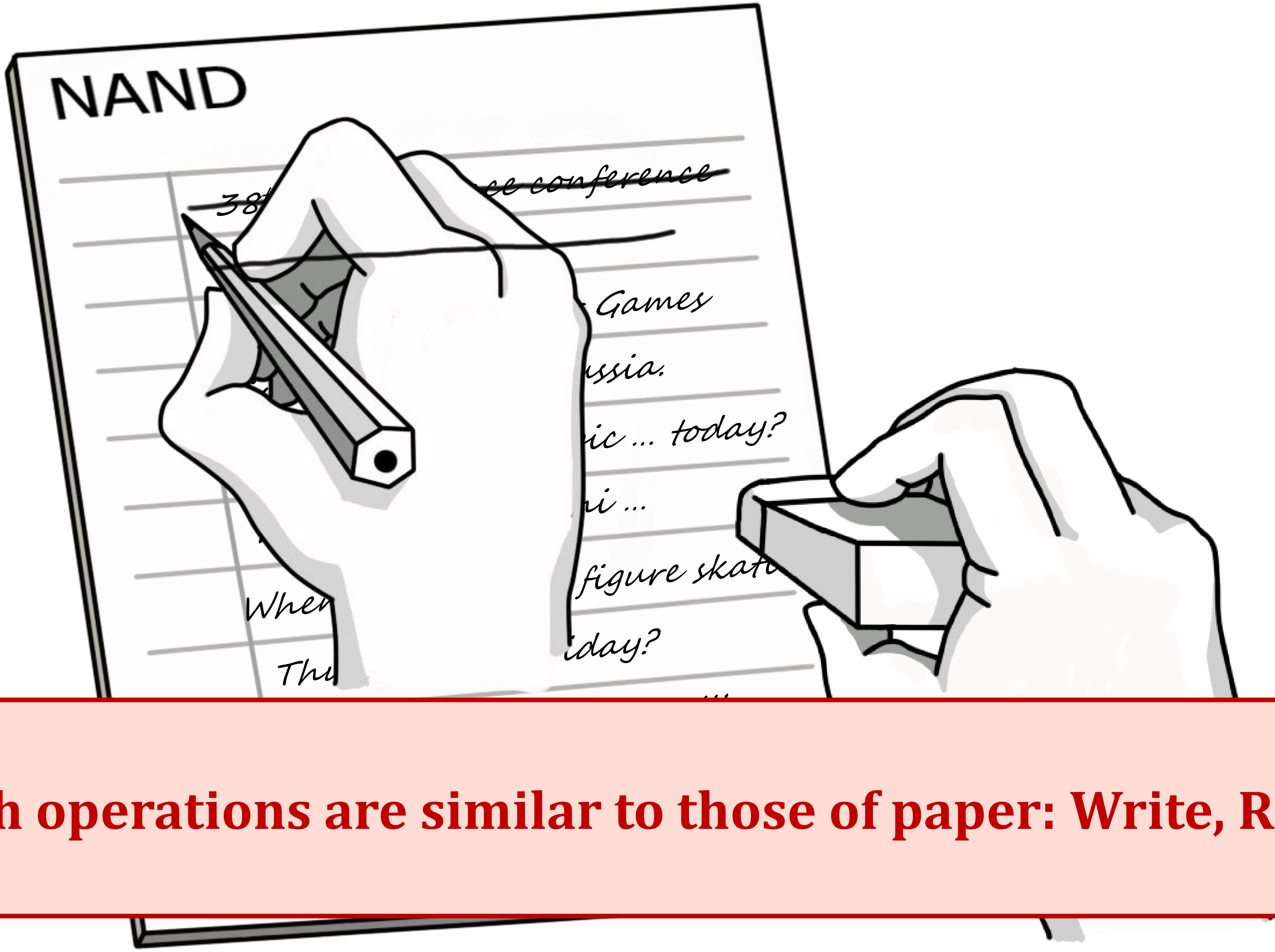
Wear Mechanism of NAND Flash Memory

- ***High operating voltage (> 20V) damages the tunnel oxide, and generates traps in the tunnel oxide***



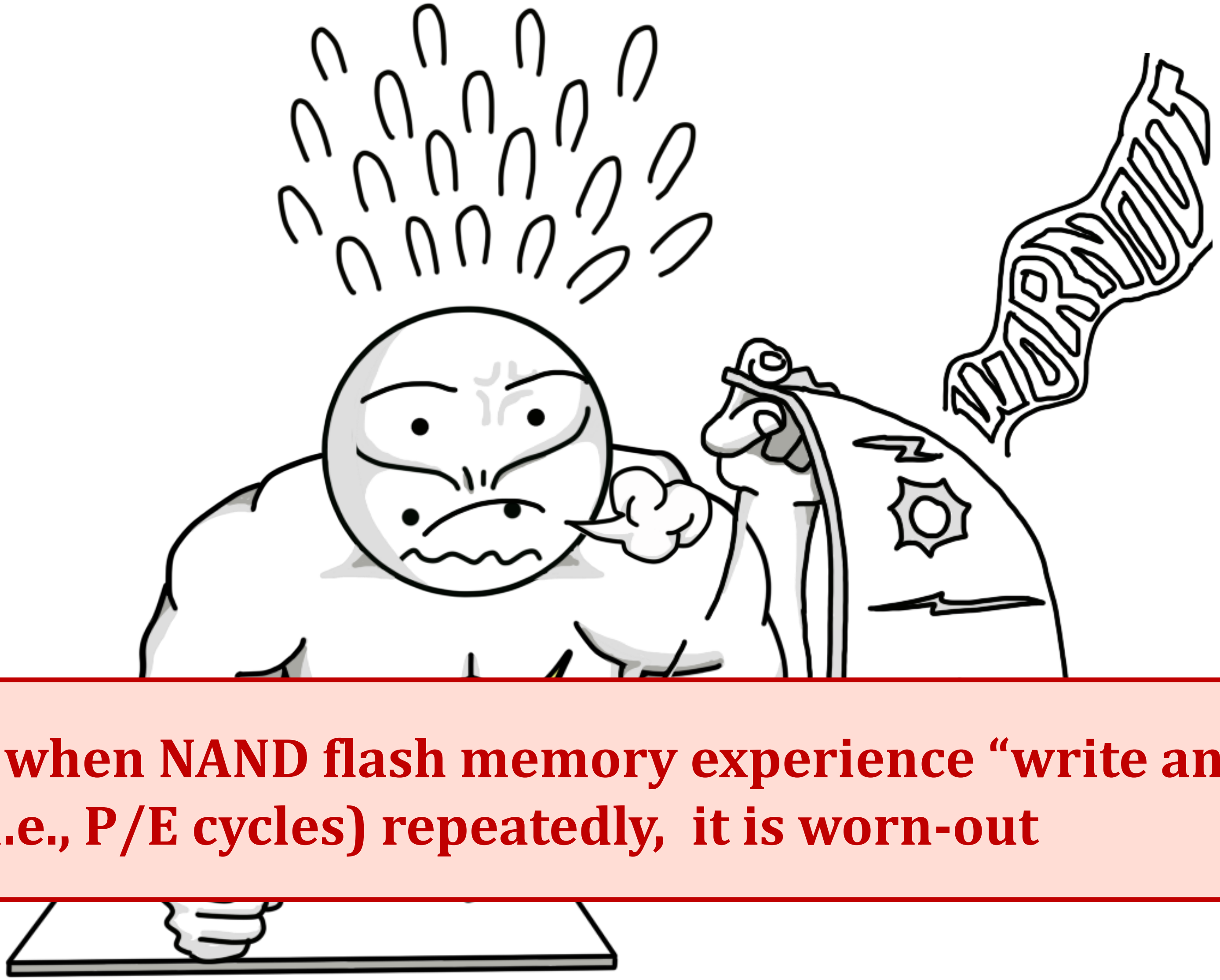
Repeated program & erase operation (P/E cycles) wear-out NAND flash memory because of tunnel oxide degradation

Wear Mechanism of NAND Flash Memory



NAND flash operations are similar to those of paper: Write, Read, Erase

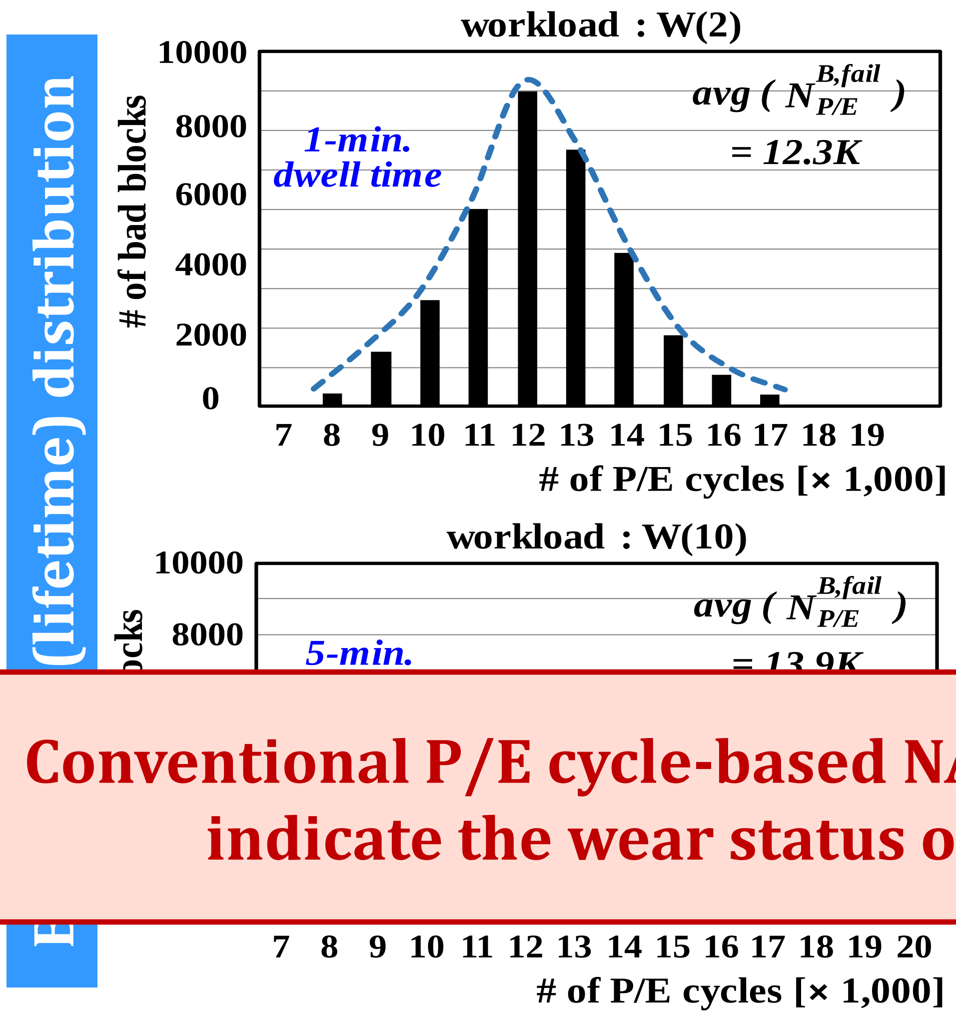
Wear Mechanism of NAND Flash Memory

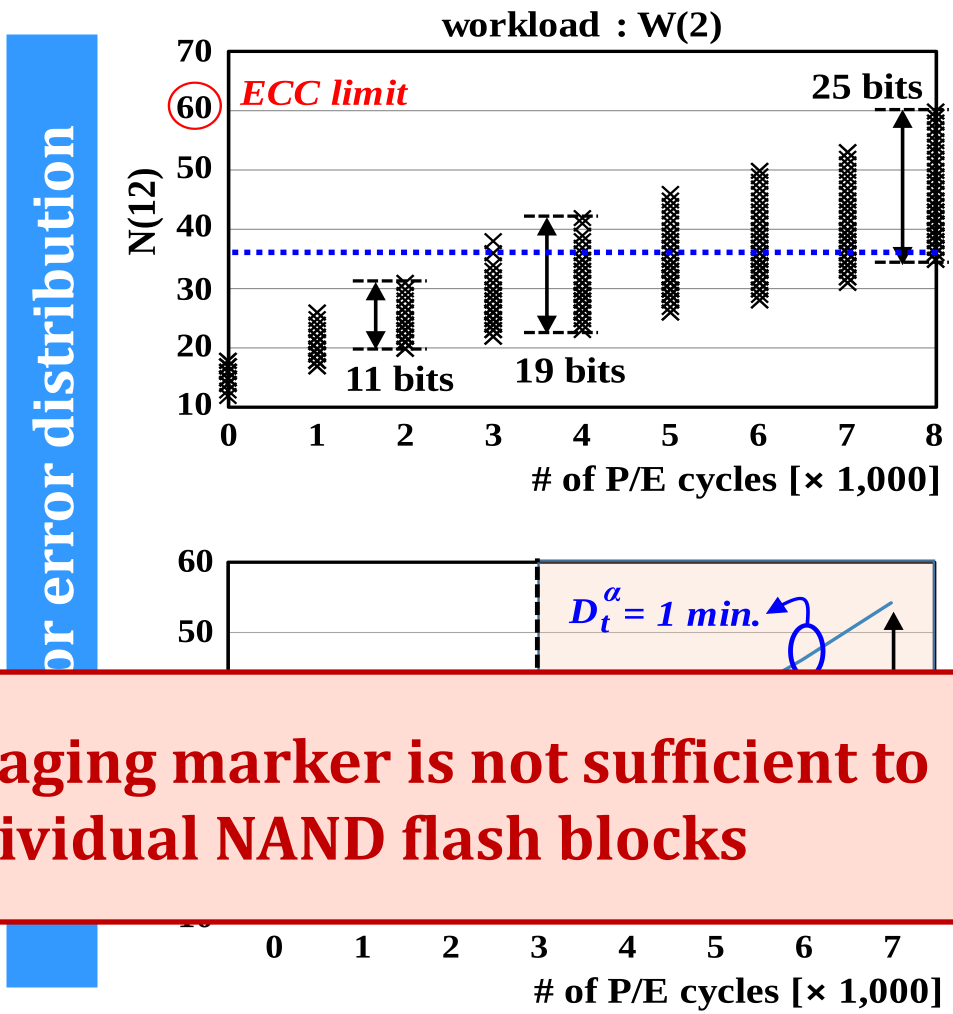


Similar to paper, when NAND flash memory experience "write and erase" (i.e., P/E cycles) repeatedly, it is worn-out

Inadequacy of P/E Cycle-based NAND Aging Marker

- ***The most common wear indicator is to count the chronological age of a NAND cell based on the number of program/erase cycles.***





Conventional P/E cycle-based NAND aging marker is not sufficient to indicate the wear status of individual NAND flash blocks

Why P/E Cycle-based NAND Aging Marker is Inadequacy?

- ***P/E cycle-based NAND aging marker is similar as the chronological age of a human being.***

Human | **NAND block**

Genetic difference (Telomere) → ***"Process variations"***

Even twins, human can exhibit different aging characteristics

Life style or living environments → ***"Operating Conditions"***

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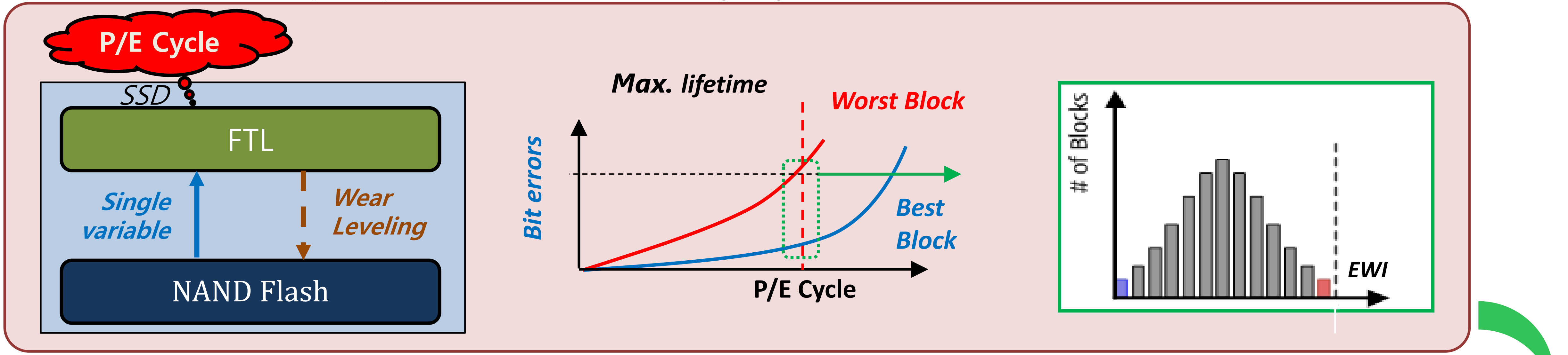
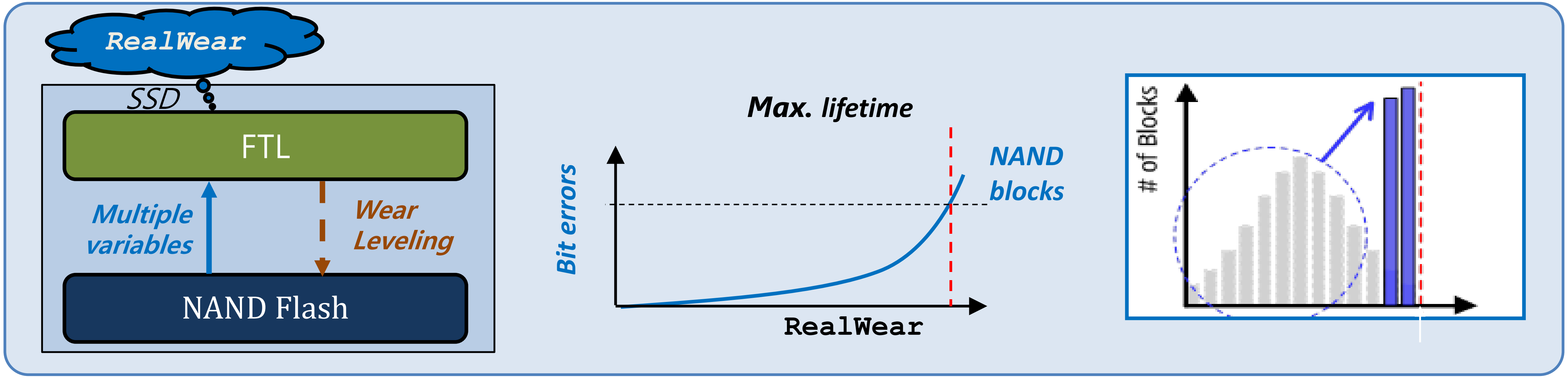
Goal of Our New NAND Aging Marker: RealWear

- Conventional P/E cycle-based NAND aging marker



- New NAND aging marker to accurately indicate the wear status of NAND blocks

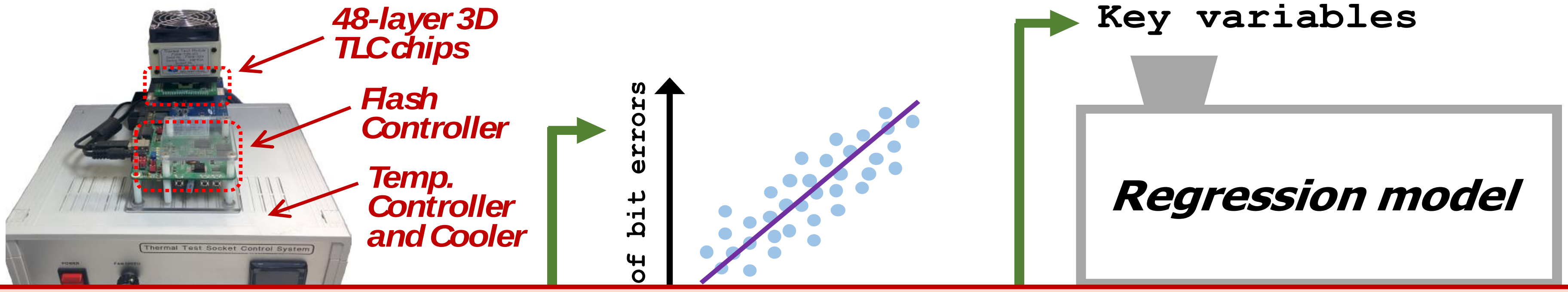


RealWear: Design Methodology

- ***RealWear considers multiple variables that are closely related to the wear-out of NAND flash memory.***
  - ✓ *Variables selection using real state-of-the-art 3D TLC flash chips + Regression model*

Phase 1:Variable Selection → **Phase 2: Building Model**

(Evaluation) **(Correlation analysis)**



We conducted the correlation test between 12-month retention bit errors after the maximum P/E cycles, N(12), cycles and each variables.

using lifetime evaluations

key variables

using a *regression model.*

RealWear: Variable Selection

- ***Investigated 10 candidate variables and selected 5 variables for RealWear based on the correlation with the wear status of flash blocks***

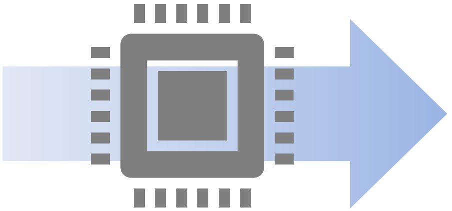
Type		*Description*	*Inclusion*
Latency	*tPROG*	*Program latency*	*X*
	tBERS	*Erase latency*	*O*
	tREAD	*Read latency*	*X*
Bit errors	*N(0)*	*# of bit errors right after program*	*O*
Noise factors	*ICI*	*Inter-Cell Interference*	*X*
	RTN	*Random Telegraph Noise*	*X*
	BPD	*Back Pattern Dependency*	*X*
Dynamic factors	$N_{P/E}$	*P/E cycles*	*O*
	D_t	*Dwell time*	*O*
	K_{amb}	*Ambient temperature*	*O*

Not correlated in high-endurance region

Difficult to on-line measure

RealWear: Building Model

- ***RealWear is constructed by multiple variables using regression model.***



$$f(x) = C_0 + \beta_1 \cdot N_{PE} + \beta_2 \cdot tBERS + \beta_3 \cdot N(0) + \beta_4 \cdot \ln(D_t^{eff})$$

Each coefficients were estimated by ***least square approximation method***.

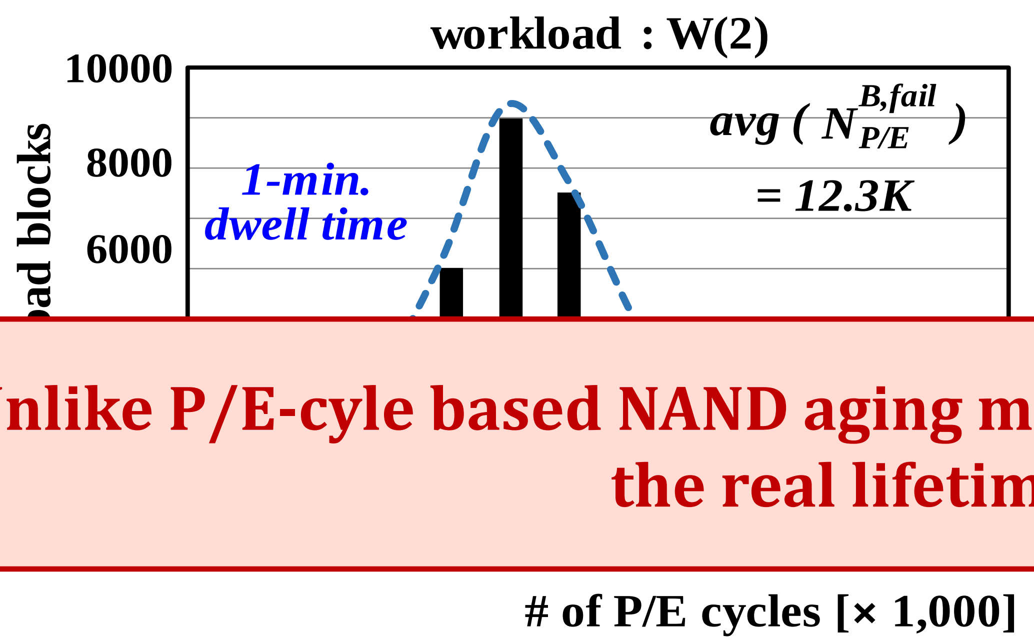
tBERS,
RBER,
# of P/E cycles
Dwell time,
Ambient temperature

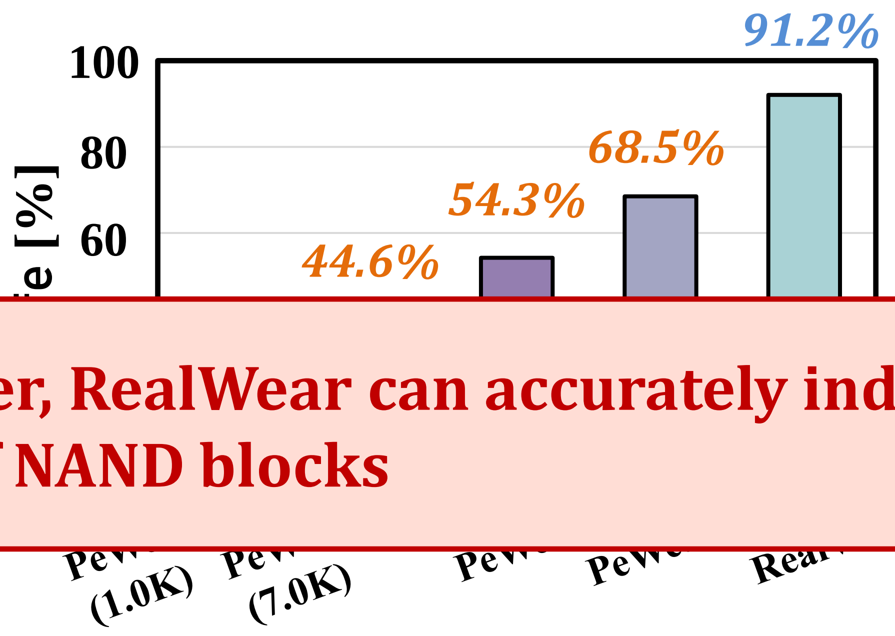
On-line measurable variables related to the wear of NAND flash memory

Model Validation: Lifetime

- ***The effectiveness of RealWear was verified over P/E cycle-based aging marker by:***
  - ✓ *1. How accurately it can estimate the lifetime of each NAND blocks*
  - ✓ *2. How effectively it can reduce the error variations between NAND blocks*
  - ✓ *3. How well it can reflect the effect of operating conditions on the wear of NAND flash memory (i.e., self-recovery effect)*

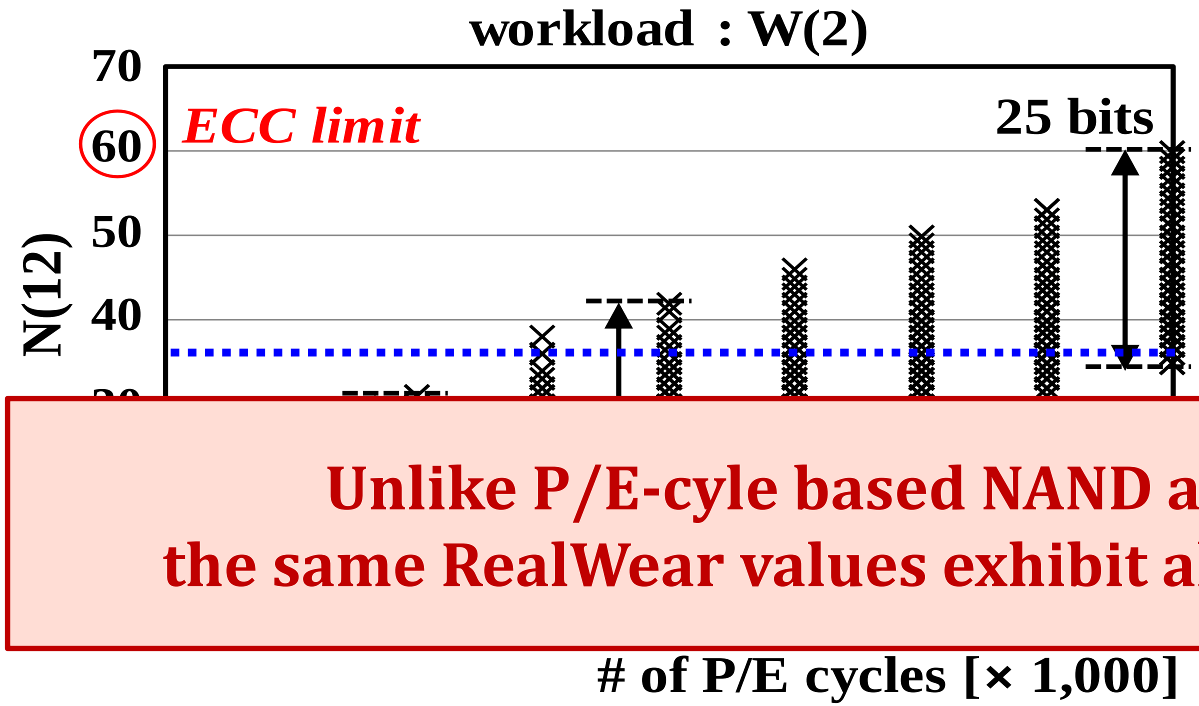
$$\texttt{Life} = \frac{\textit{Predicted total amounts of writes}}{\textit{Actual total amounts of writes}} \times 100$$

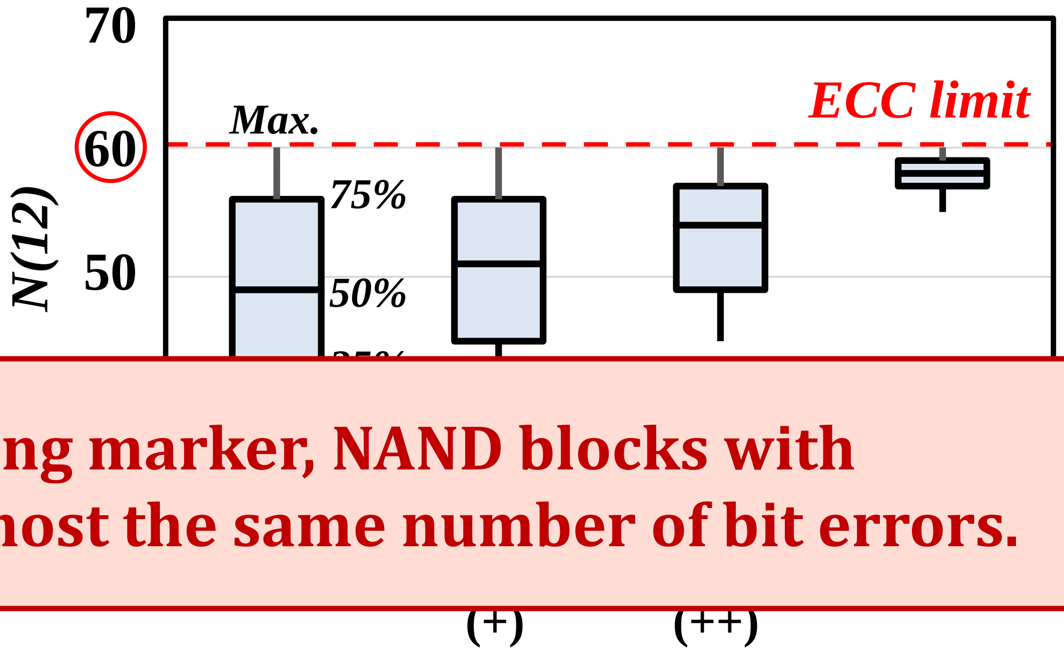




Unlike P/E-cyle based NAND aging marker, RealWear can accurately indicate the real lifetime of NAND blocks

- *The effectiveness of RealWear was verified over P/E cycle-based aging marker by:*
  - ✓ ***2. How effectively it can reduce the error variations between NAND blocks***

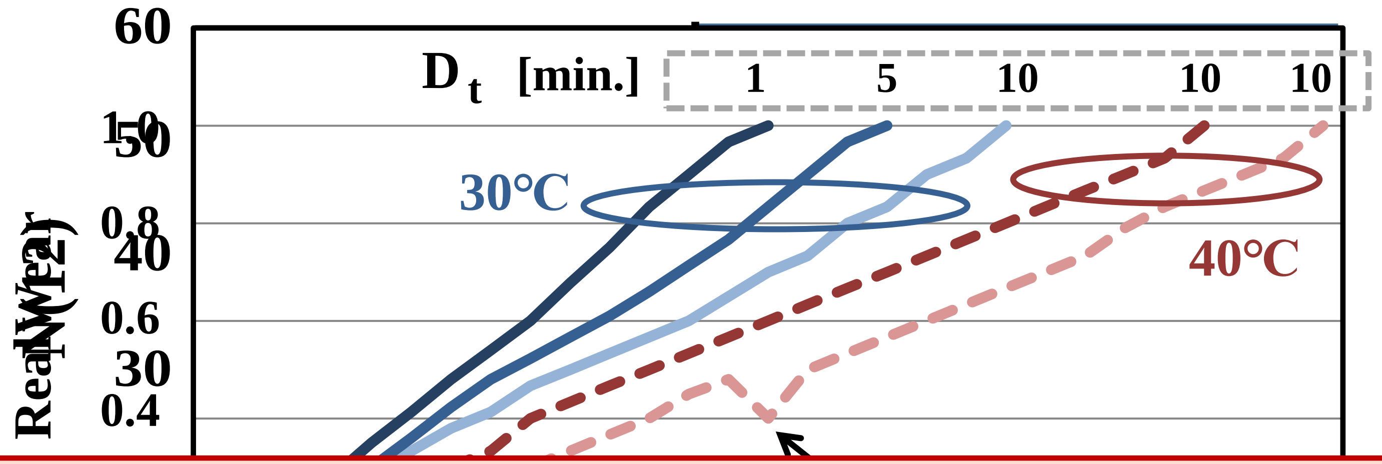




Unlike P/E-cyle based NAND aging marker, NAND blocks with the same RealWear values exhibit almost the same number of bit errors.

Model Validation: Operating Condition Effects

- *The effectiveness of RealWear was verified over P/E cycle-based aging marker by:*
  - ✓ ***3. How well it can reflect the effect of operating conditions on the wear of NAND flash memory (i.e., self-recovery effect)***



Unlike P/E-cyle based NAND aging marker, RealWear properly reflects the impact of I/O workload variation and temperature variation on the wear of NAND blocks.

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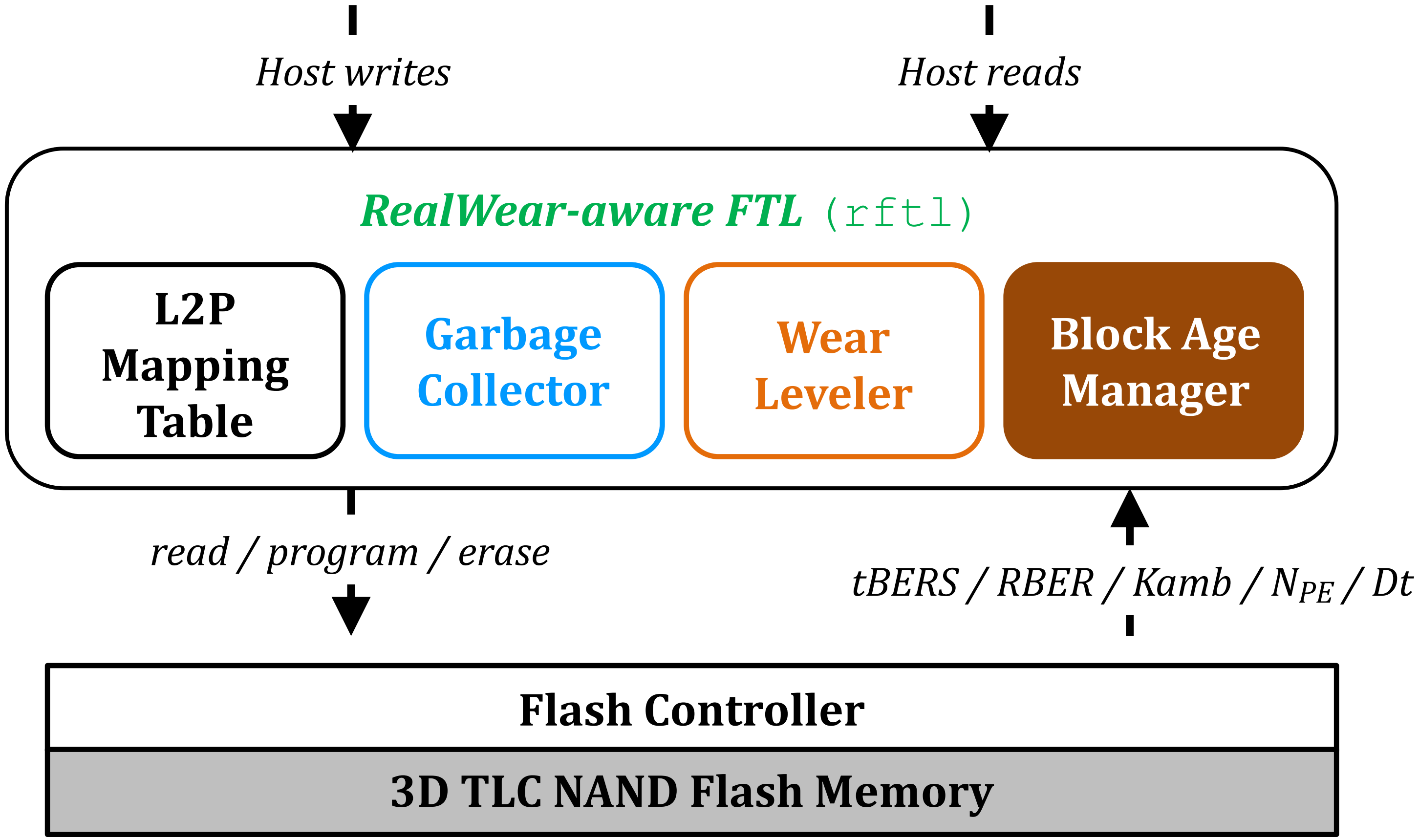
Experiment Settings

- ***RealWear-aware flash transition layer*** **(`rftl`) is implemented based on a flash emulation environment.**



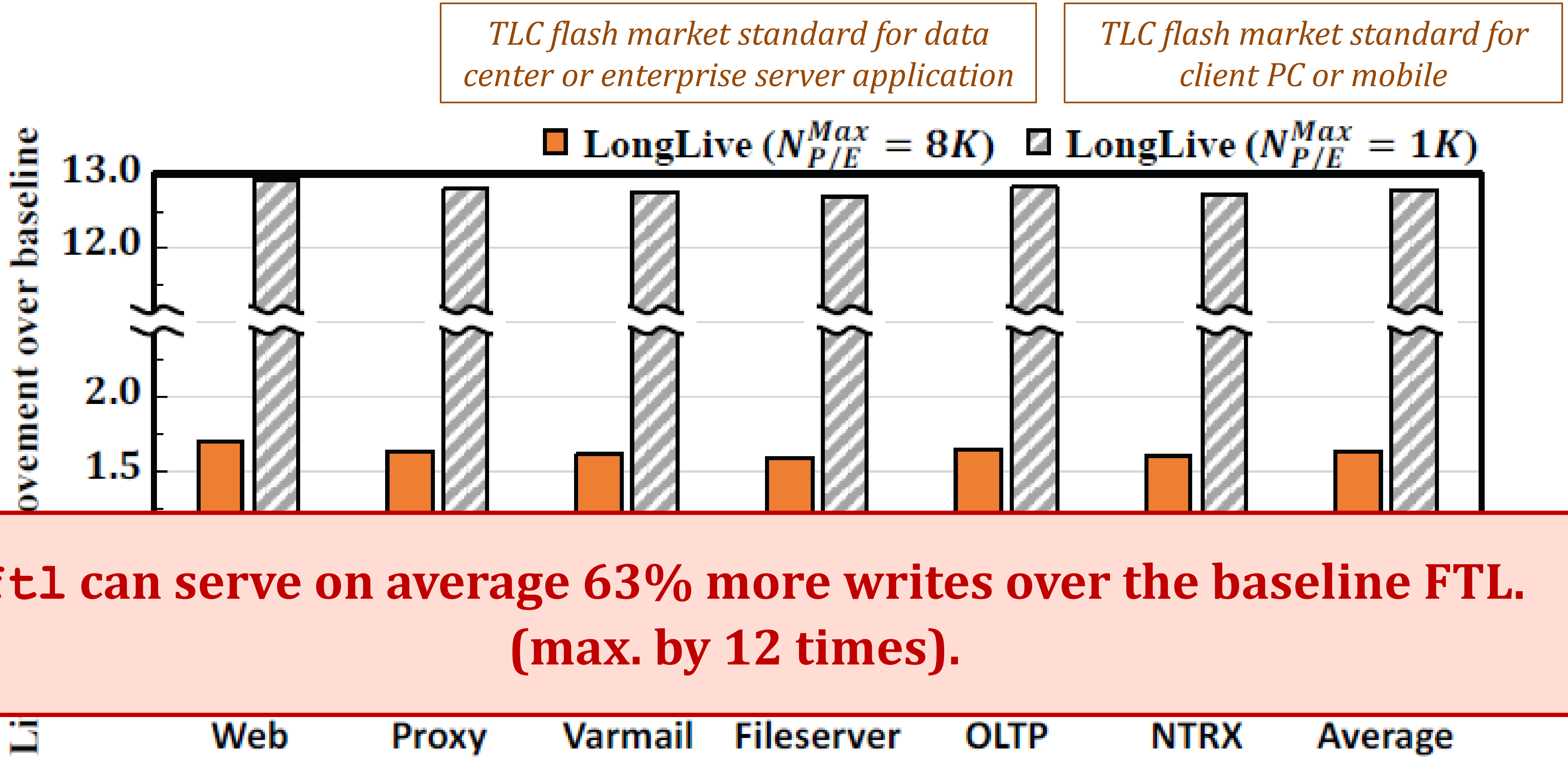
- 576 pages per block
- 16-KiB page size

(Characteristics of six workload)

Wrokload	Read:Write	WAF
`Varmail`	40:60	2.7
`Fileserver`	40:60	5.4
`Proxyserver`	55:45	1.9
`Webserver`	85:15	1.2
`OLTP`	70:30	2.0
`NTRX`	5:95	2.3

Case Study 1 : Lifetime

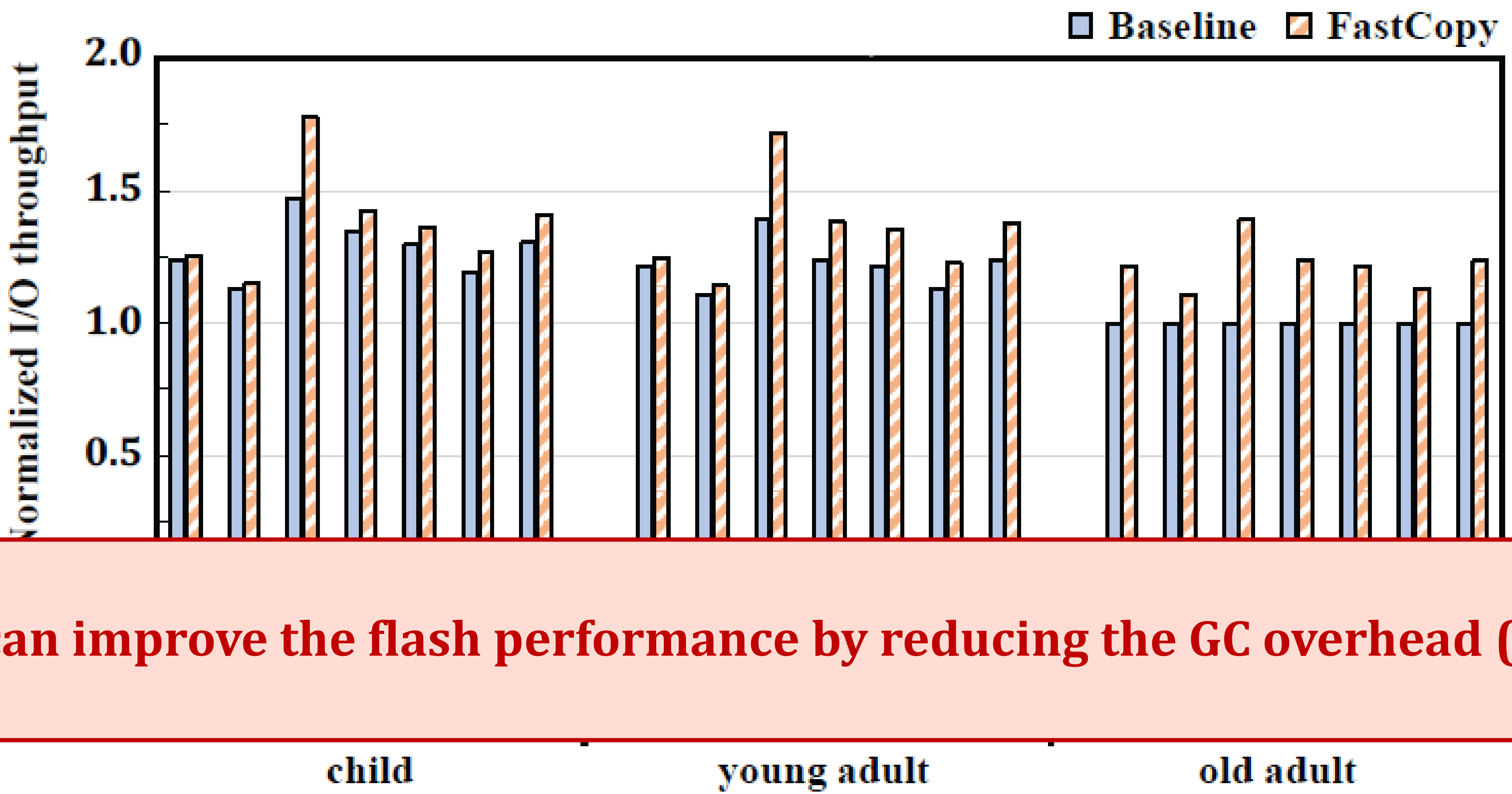
- ***We measured the total amount of writes until an SSD reaches the end of its lifetime.***



`rftl` can serve on average 63% more writes over the baseline FTL. (max. by 12 times).

Case Study 2 : Performance (Overhead of Garbage Collection)

- `rftl` *can maximize the effect of the existing optimization technique.*

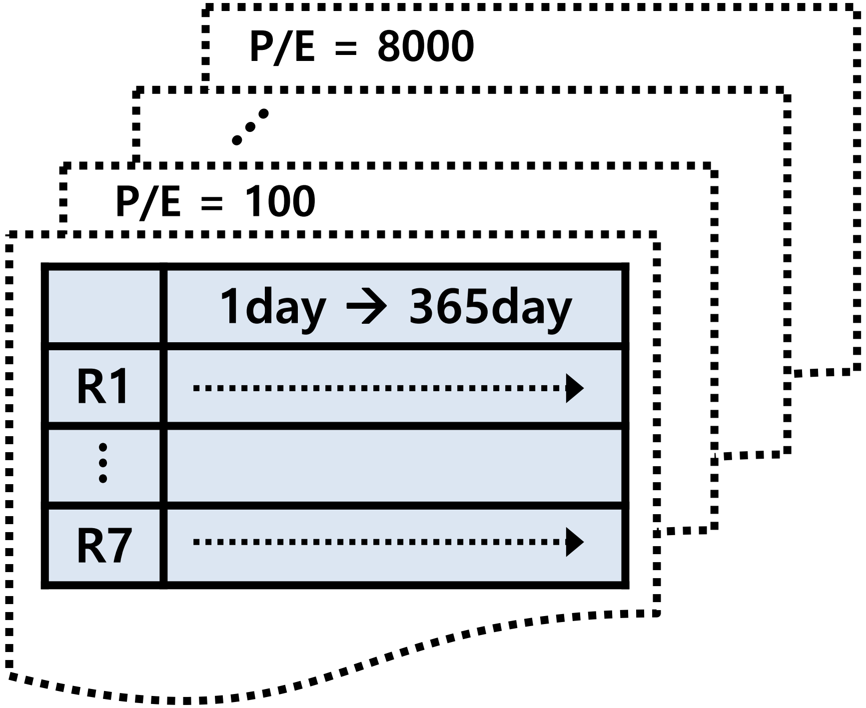


`rftl` can improve the flash performance by reducing the GC overhead (~21%)

Case Study 3 : BoundedRead (Read latency Improvement)

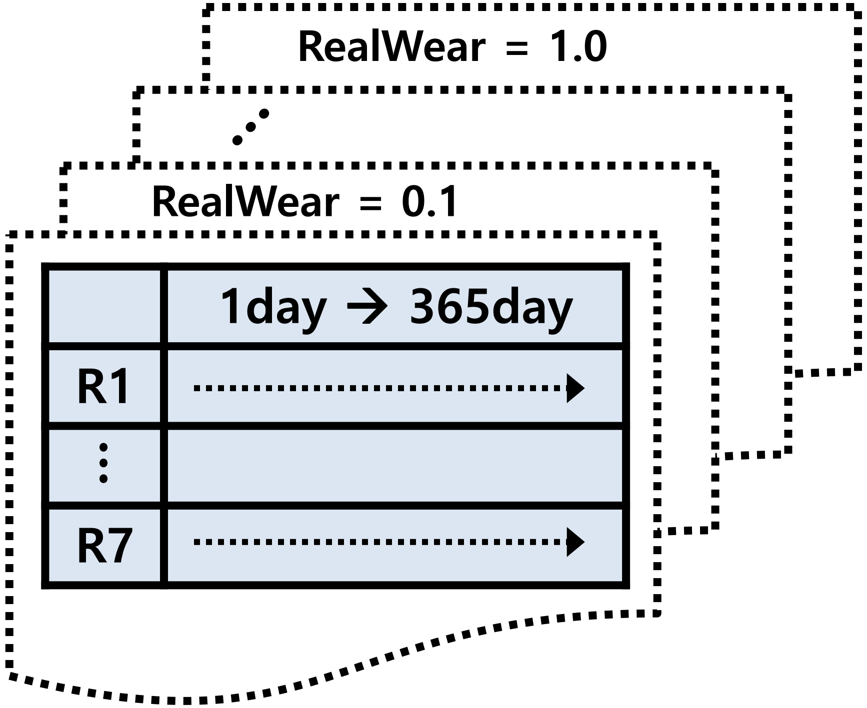
- ***To minimize the fluctuations in read latency, the optimal read reference voltage is provided as look-up table depending on the wear status of NAND blocks.***

ORT_pe
*(optimal read reference table based on **# of P/E cycles**)*



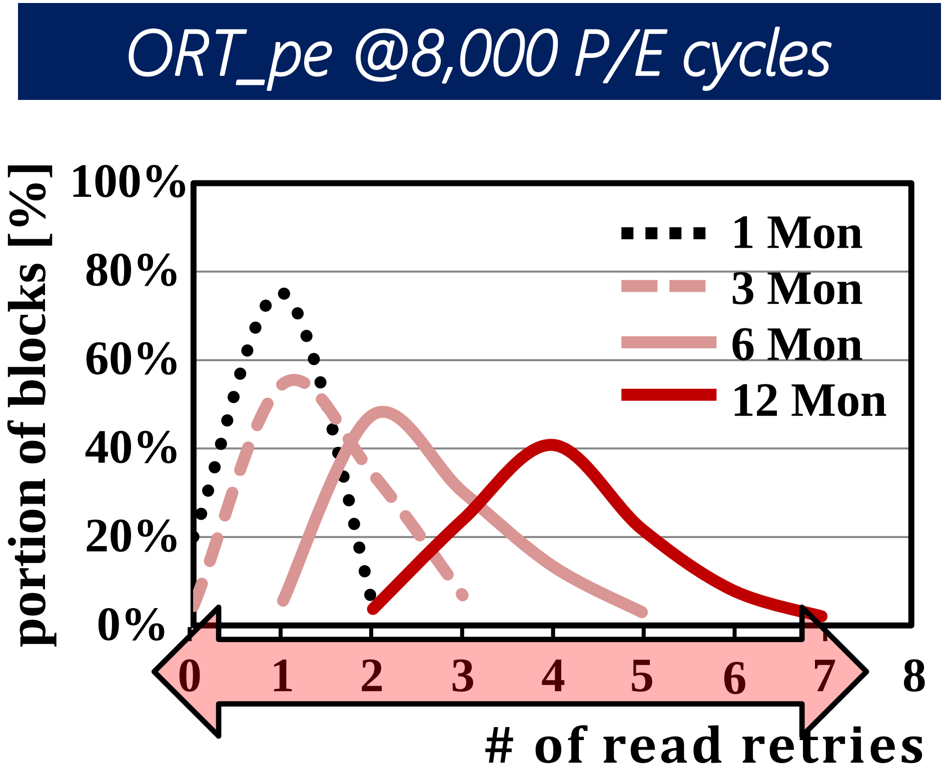
VS.

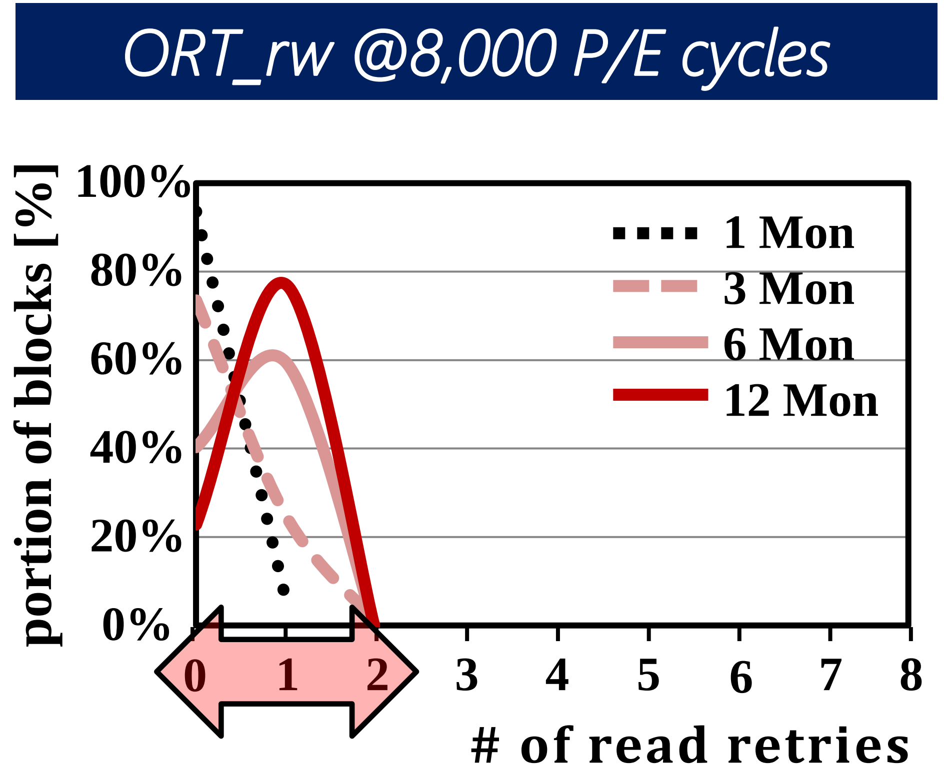
ORT_pe
*(optimal read reference table based on **RealWear**)*



Case Study 3 : BoundedRead (Read latency Improvement)

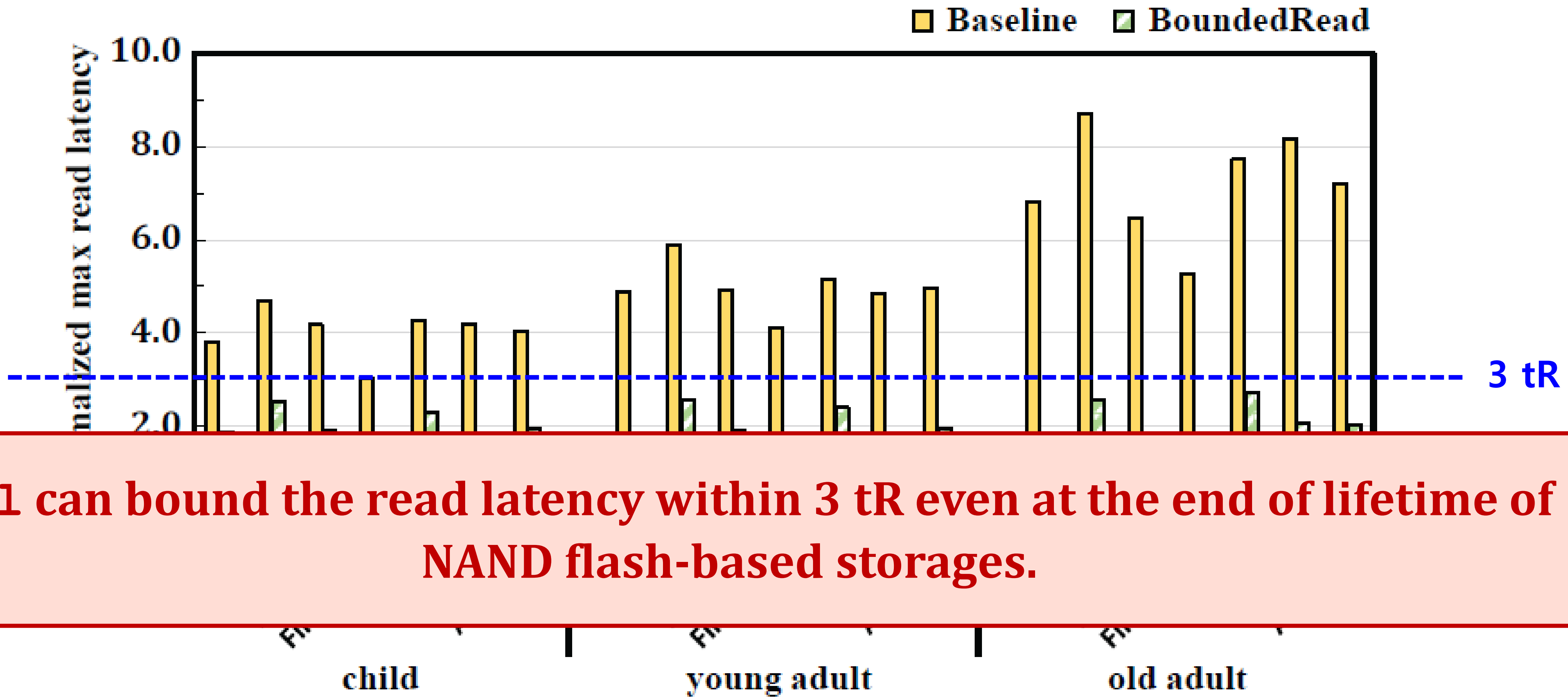
- ***In ORT_rw, no blocks need more than 2 read retries regardless of the data retention requirement.***
  - ✓ *Using 160 read 3D TLC flash chips*





Case Study 3 : BoundedRead (Read latency Improvement)

- `rftl` *can effectively mitigate the fluctuations in read latency*



`rftl` can bound the read latency within 3 tR even at the end of lifetime of NAND flash-based storages.

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Conclusions

- **Conventional P/E cycle-based NAND aging marker is not sufficient to indicate the wear status of NAND flash memory**

  → Process variation between NAND blocks & different operating conditions

- **Presented a new NAND aging marker, RealWear, and verified its adequacy by comparing it with other existing NAND aging markers.**
  - Implemented using multiple NAND parameters & validated using read 160 3D TLC flash chips
  - Improving lifetime (63% on average, max 12 times), reducing GC overhead (21%), and mitigating the read latency fluctuations

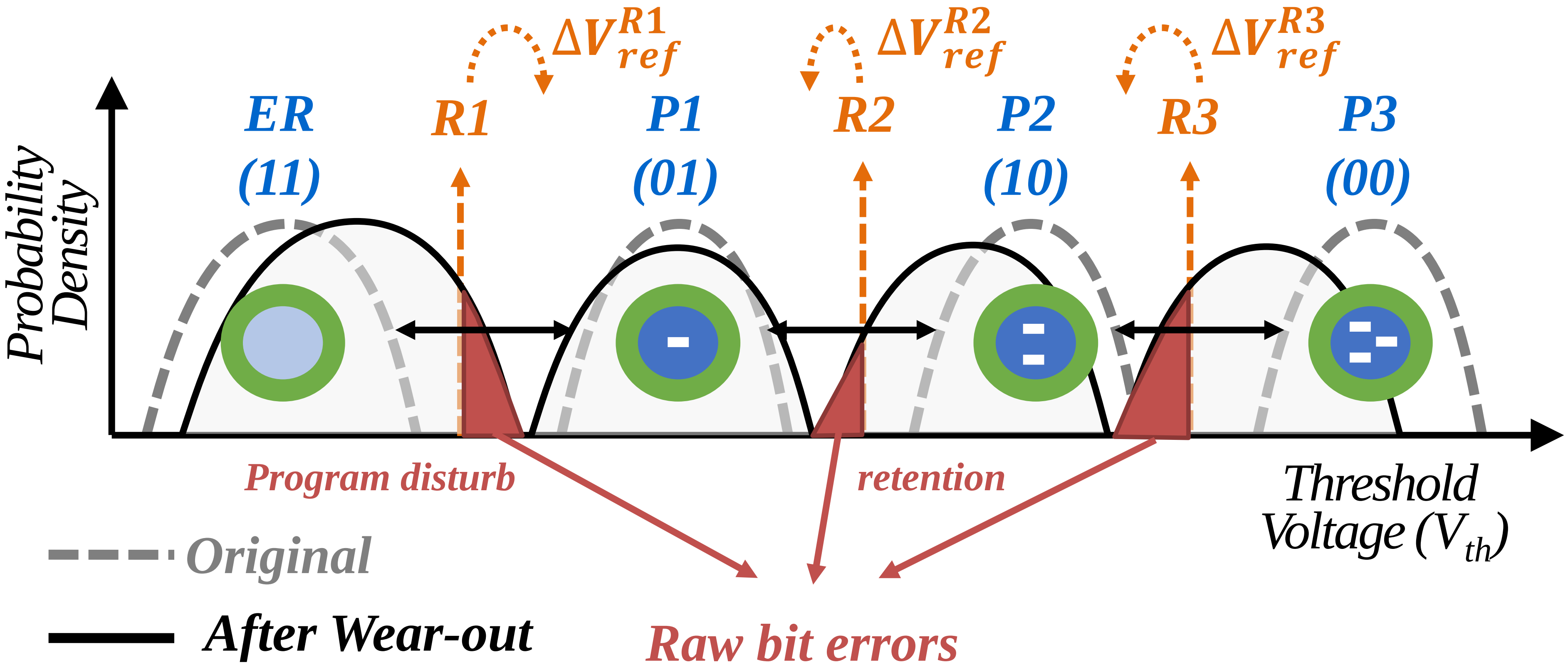
- **Future Directions**
  - ML-based Aging Marker Development
  - Real-Time SSD based on Bounded Reads

Thank You!

Appendix

Bit Errors Due to Wear of NAND Flash Memory

- ***As NAND flash memory wear-out, Vth distributions of the NAND flash cells are widen and shifted, thus generating NAND bit errors.***
  - ✓ *NAND bit errors cause a long read latency due to read retires*
  - ✓ *If NAND bit errors exceeds ECC capability even after read retries, NAND blocks is regarded as bad block (failure)*



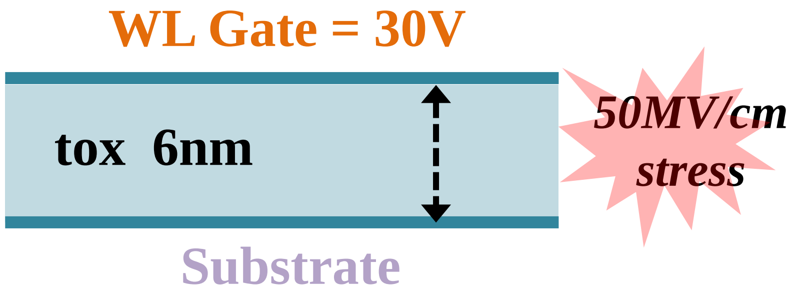
Why P/E Cycle-based NAND Aging Marker is Inadequacy?

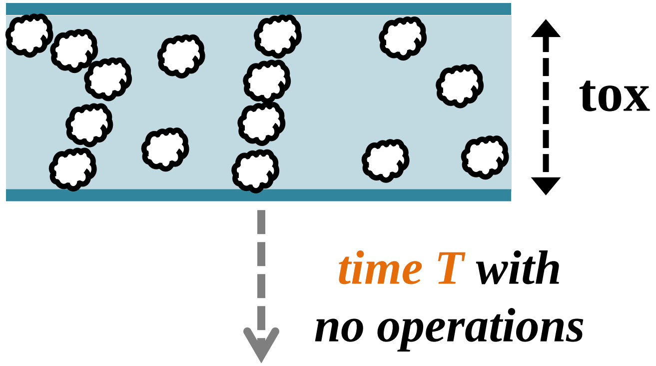
- *There are several factors to affect the wear status of NAND flash memory*

Process variation effect

I/O workload & Operating environment effect

NAND cell (a)





WL Gate = 30V

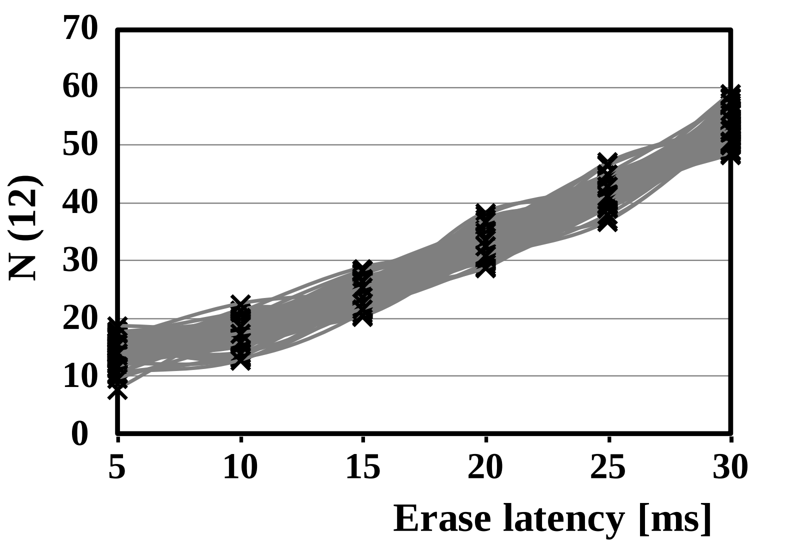
To reflect various factors to cause difference aging characteristics in NAND blocks, we propose a new NAND aging marker.

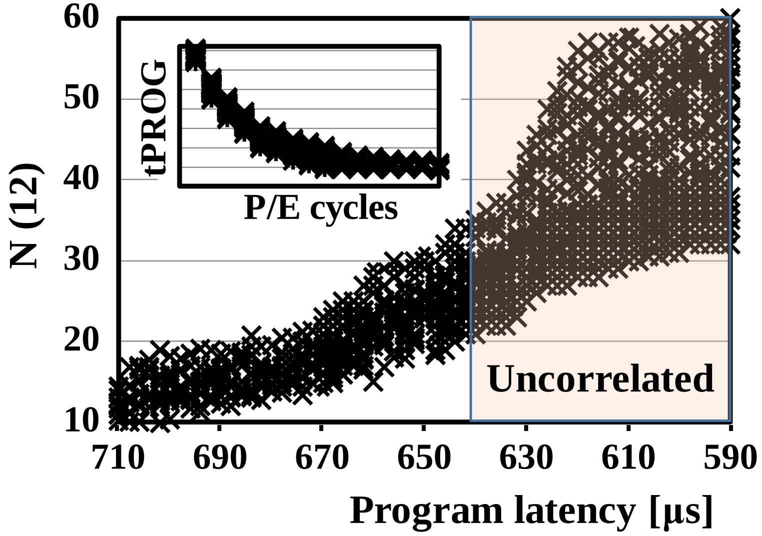
wear-out

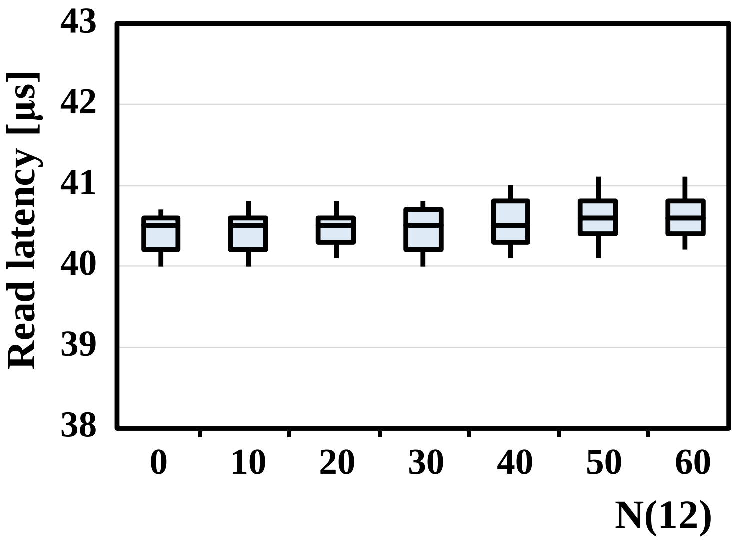
Traps are degenerated by thermal energy

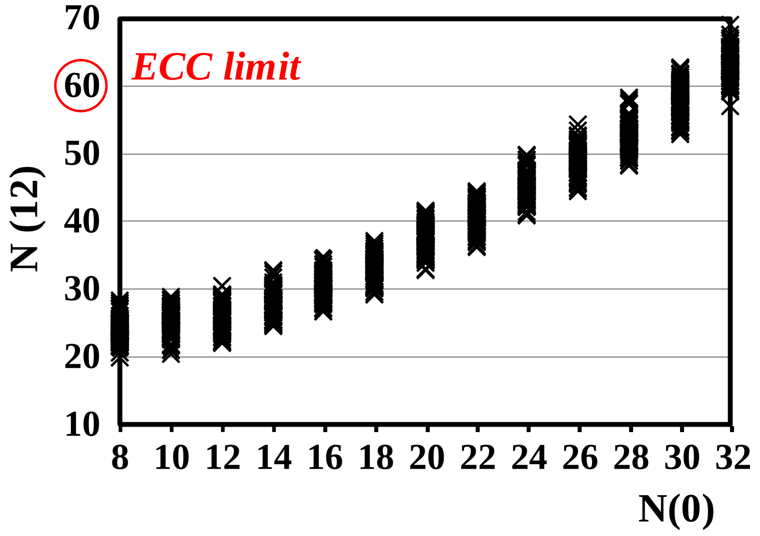
“Self-Recovery Effect”

The Results of Correlation Test









The Results of Correlation Test